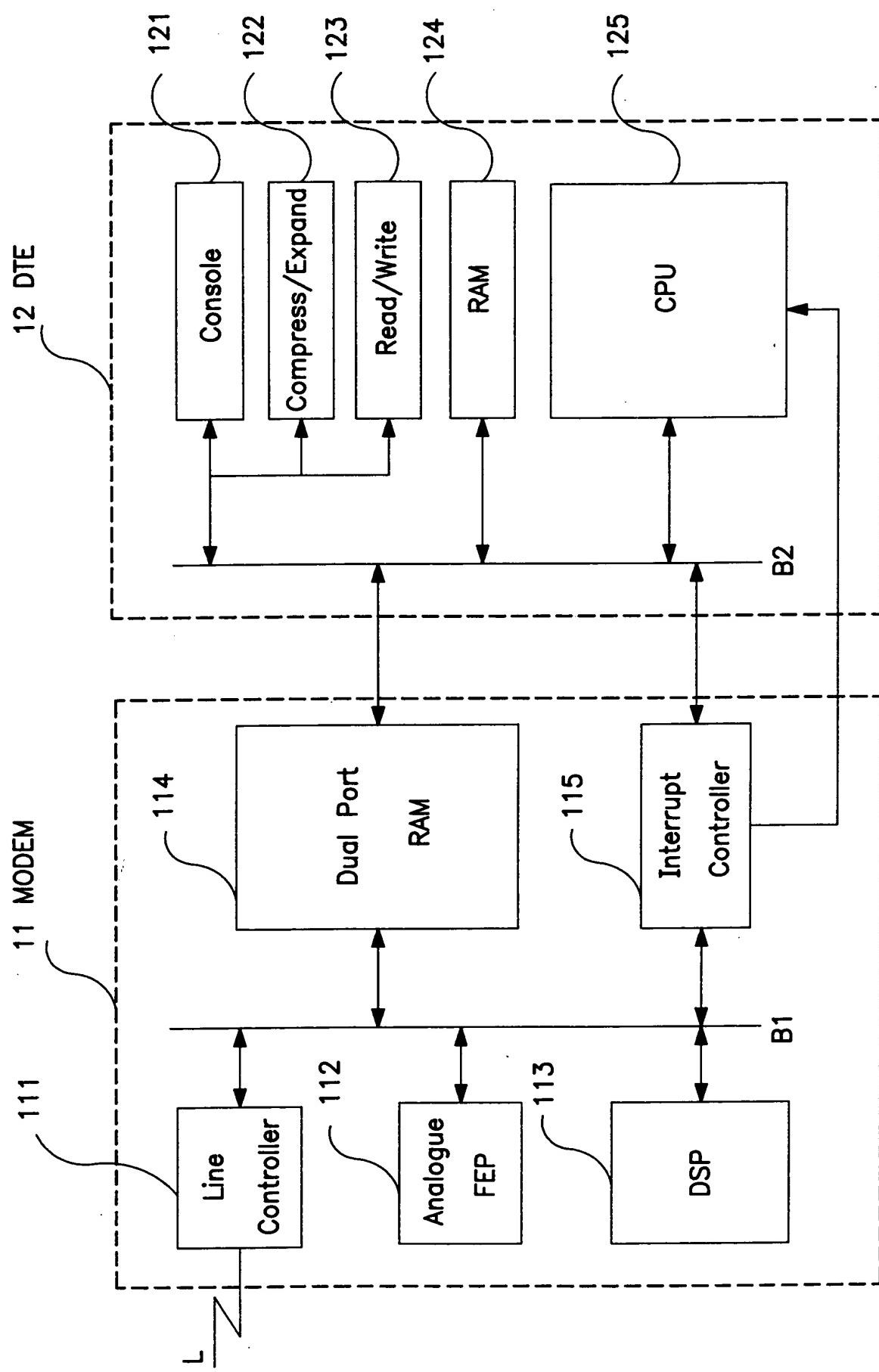


FIG. I



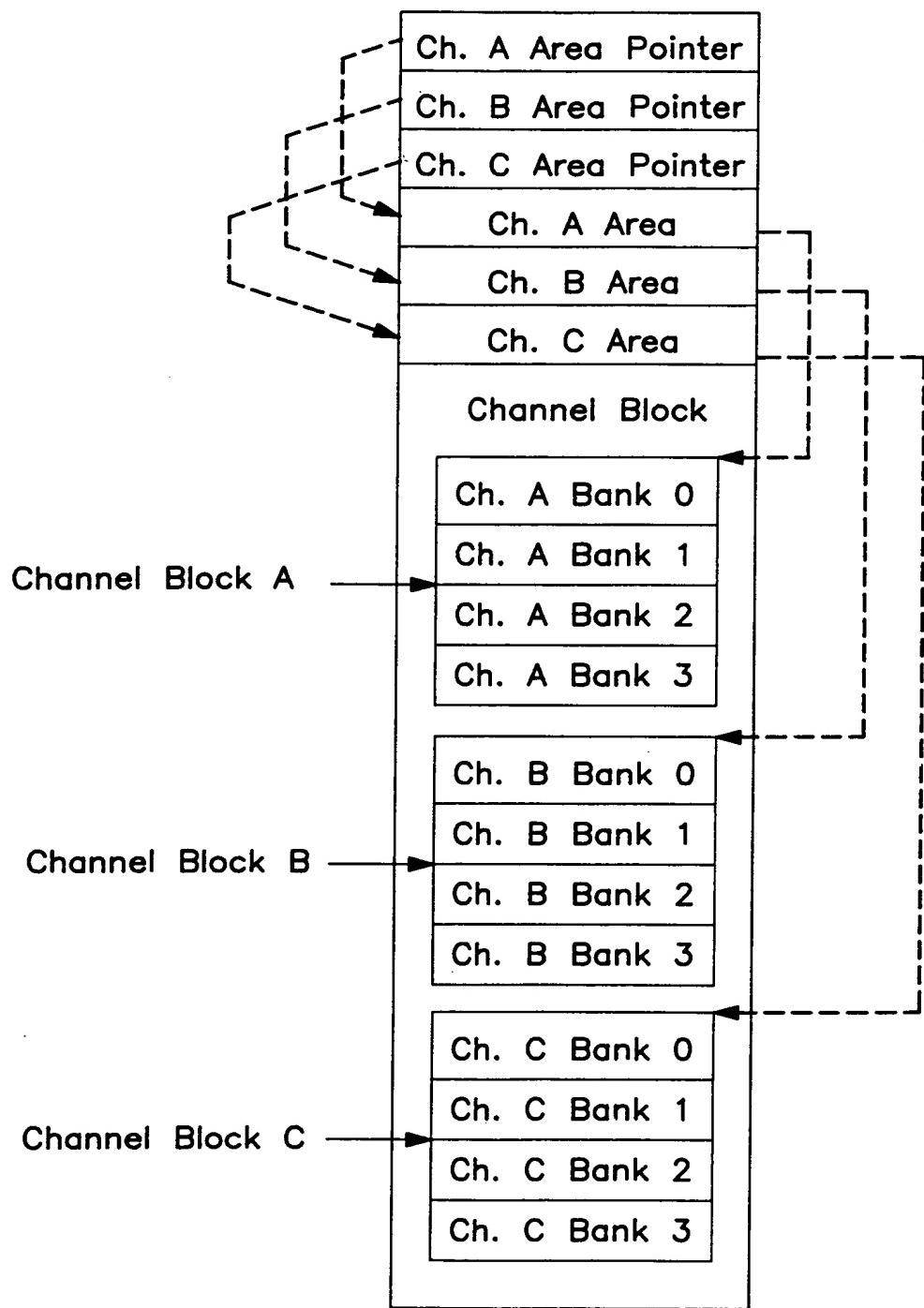


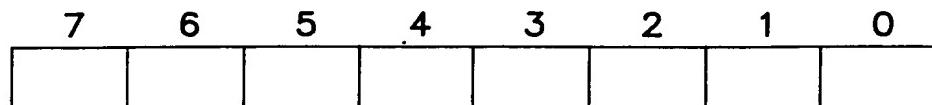
FIG. 2

Channel Area

Channel Command
Channel Status
Bank 0 Top Address
Bank 0 End Address
Bank 1 Top Address
Bank 1 End Address
Bank 2 Top Address
Bank 2 End Address
Bank 3 Top Address
Bank 3 End Address

FIG. 3

Channel Command



→ Channel Mode

0: receiving mode

1: transmitting mode

FIG. 4

Channel Status

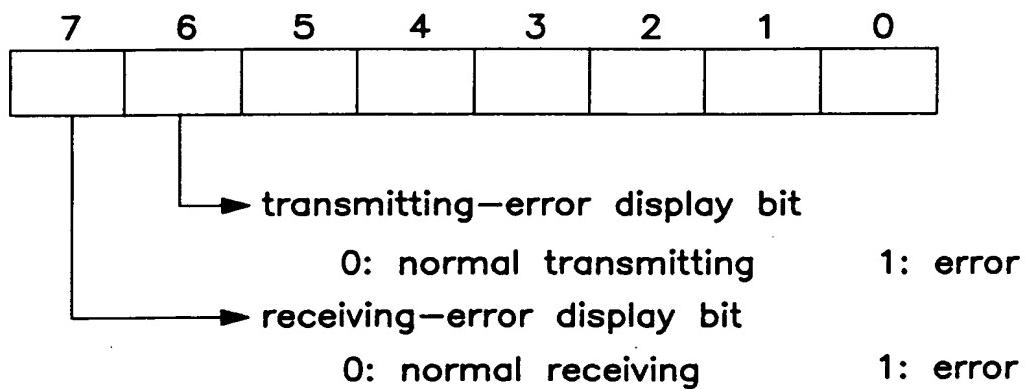


FIG. 5

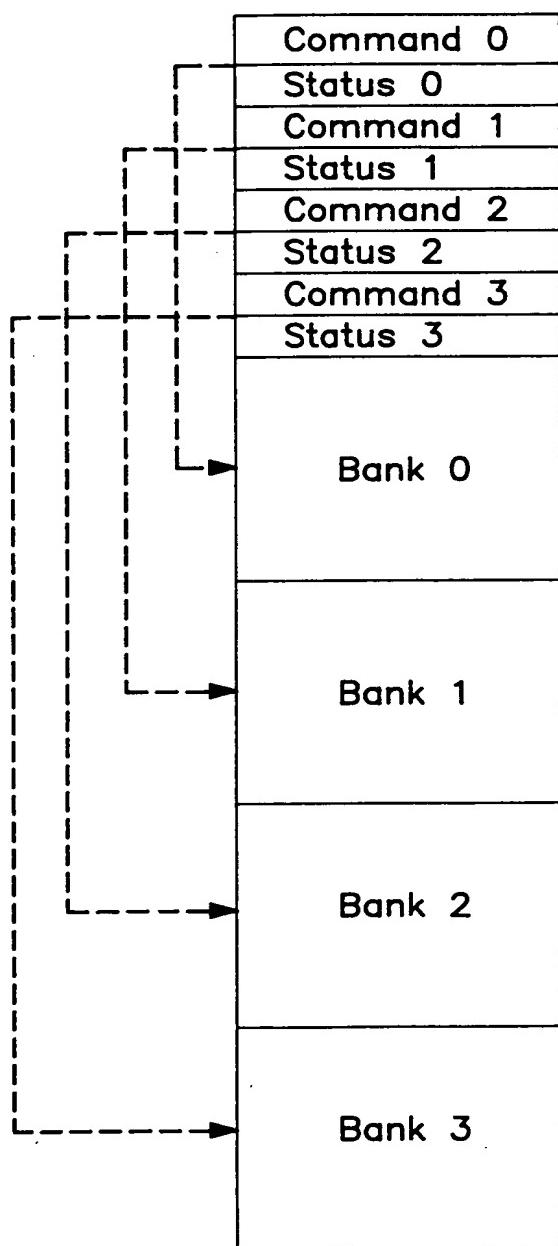
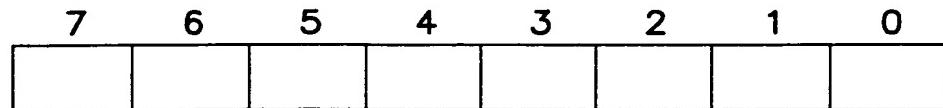


FIG. 6

Channel 0



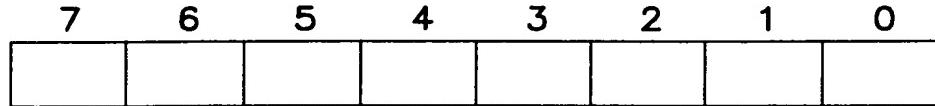
→ End-instruction bit to each channel

0: not end

1: end

FIG. 7

Status 0



→ FCS NG

0: FCS OK

1: FCS NG

→ Abort occurs

0: no abort in this bank

1: abort exists in this bank

→ Data Full/Empty display bit

0: Read end = Write enable

1: Write end = Read enable

FIG. 8

Transmitting Interrupt Status

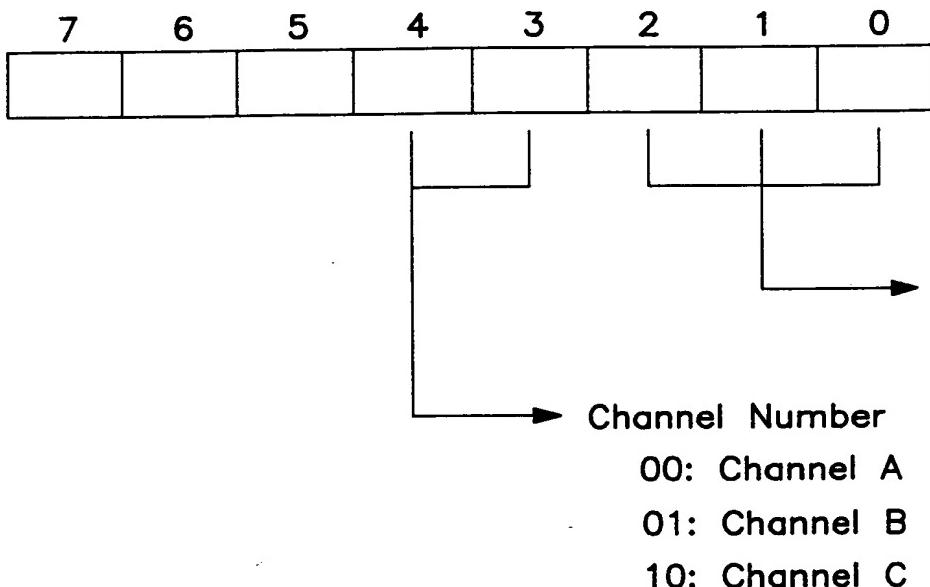


FIG. 9

Receiving Interrupt Status

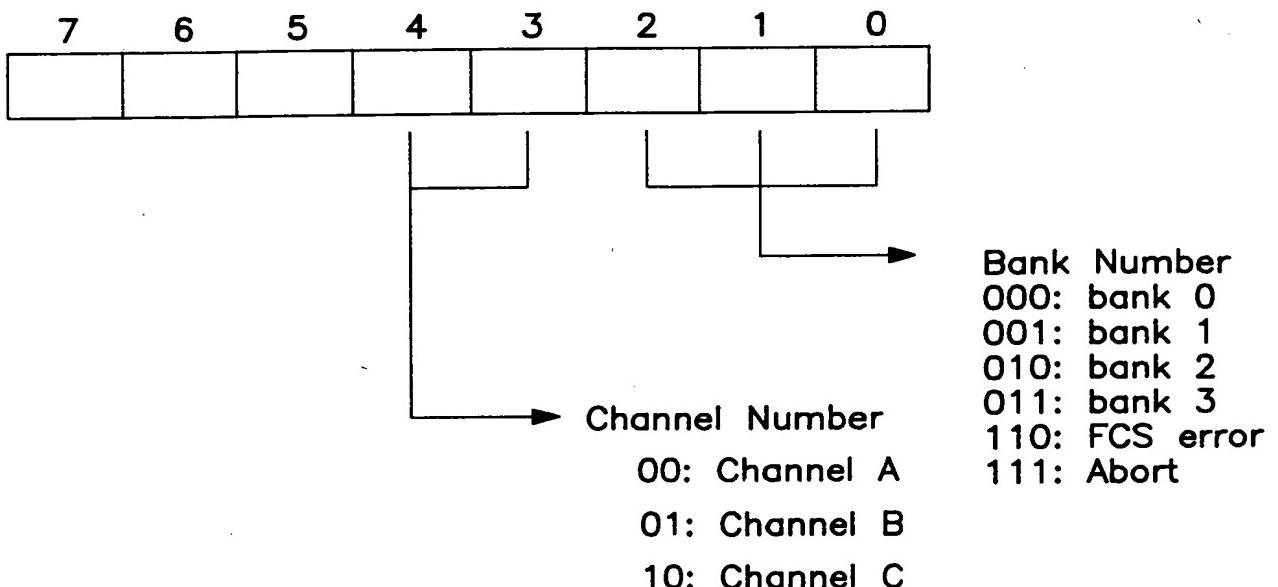


FIG. 10

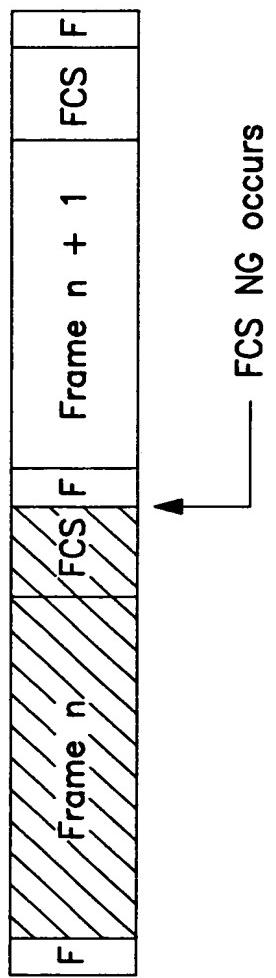


FIG. 11

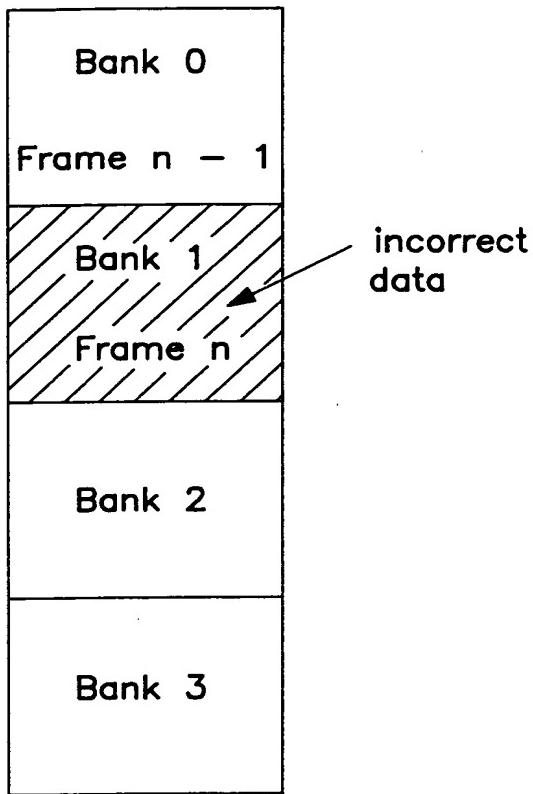


FIG. I2 (a)

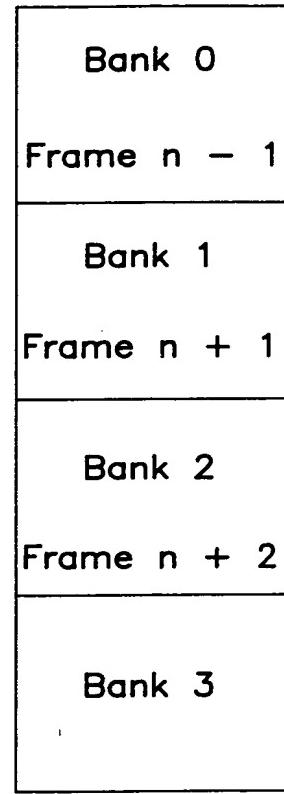


FIG. I2 (B)

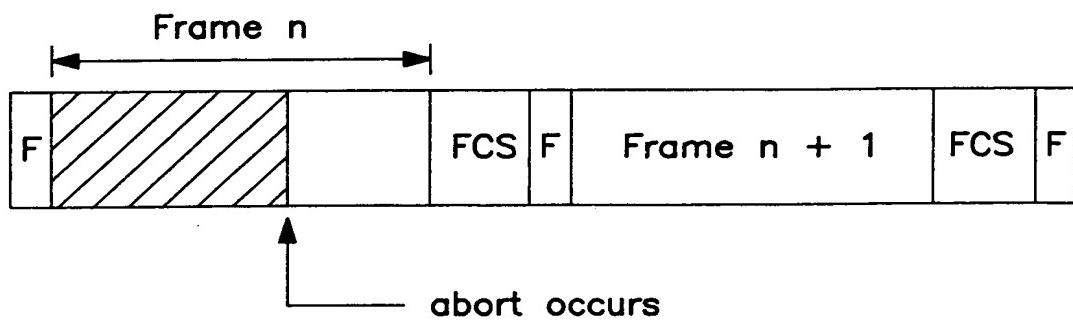


FIG. I3

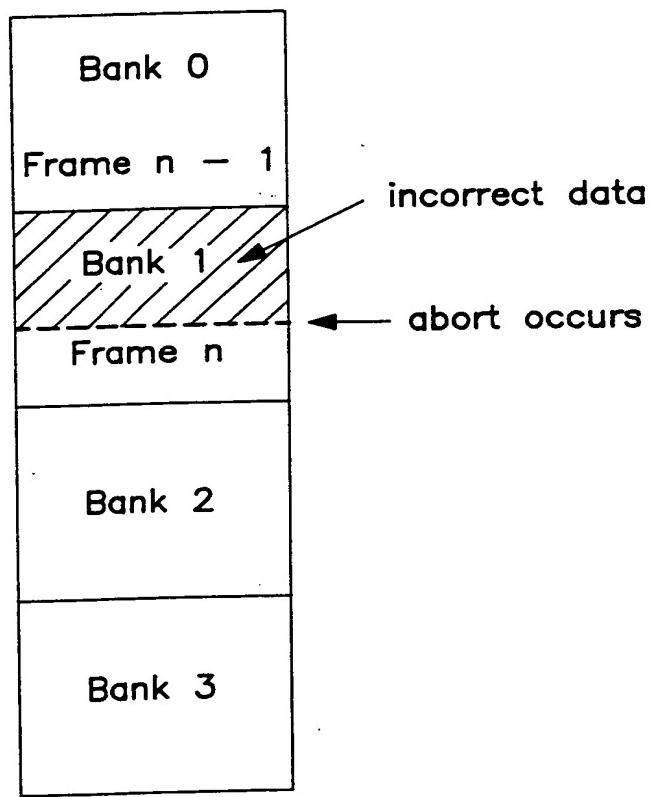


FIG. 14 (a)

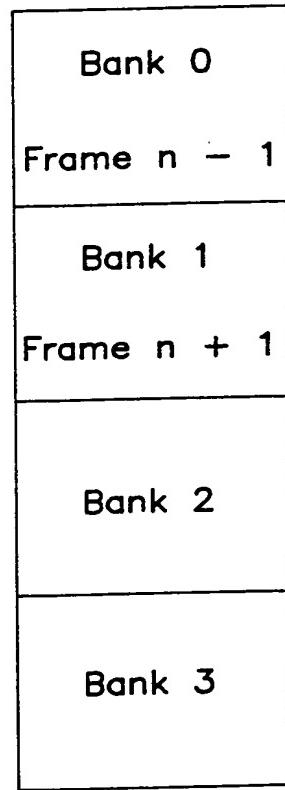


FIG. 14 (B)

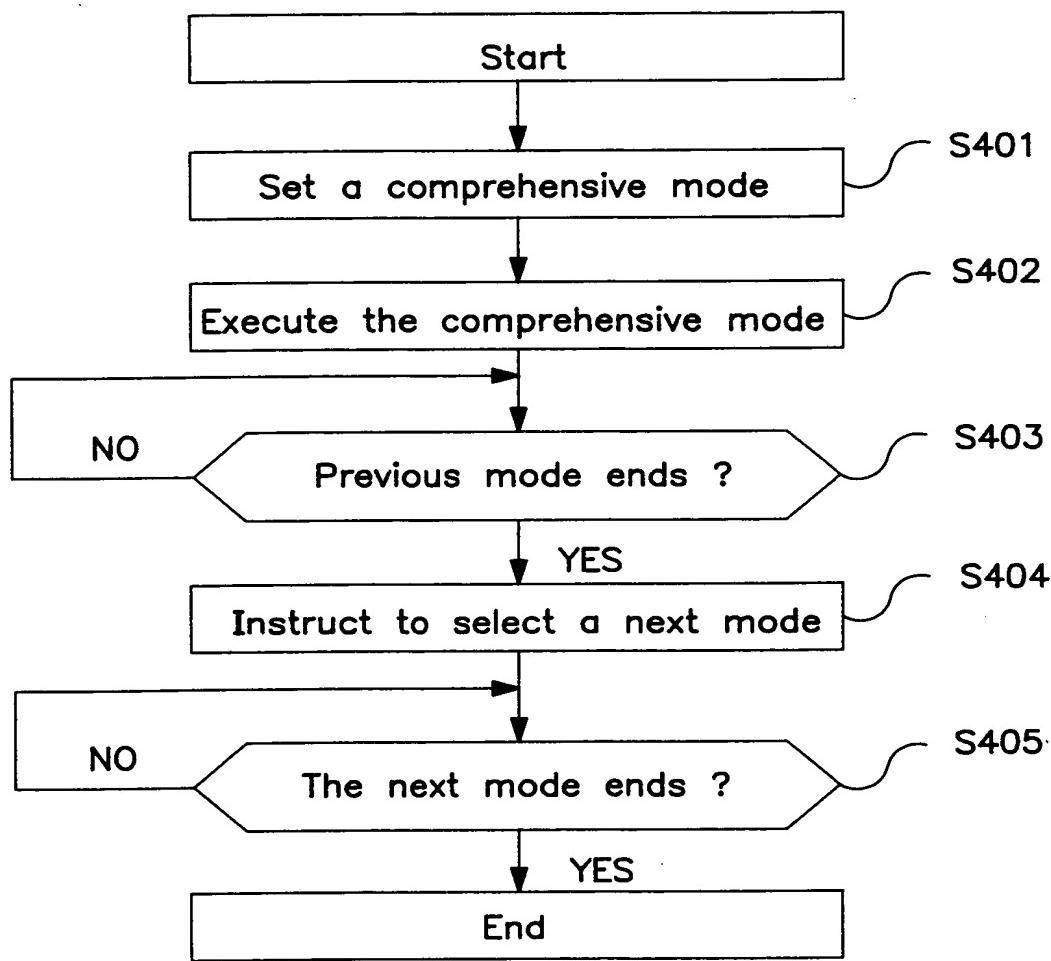


FIG. 15

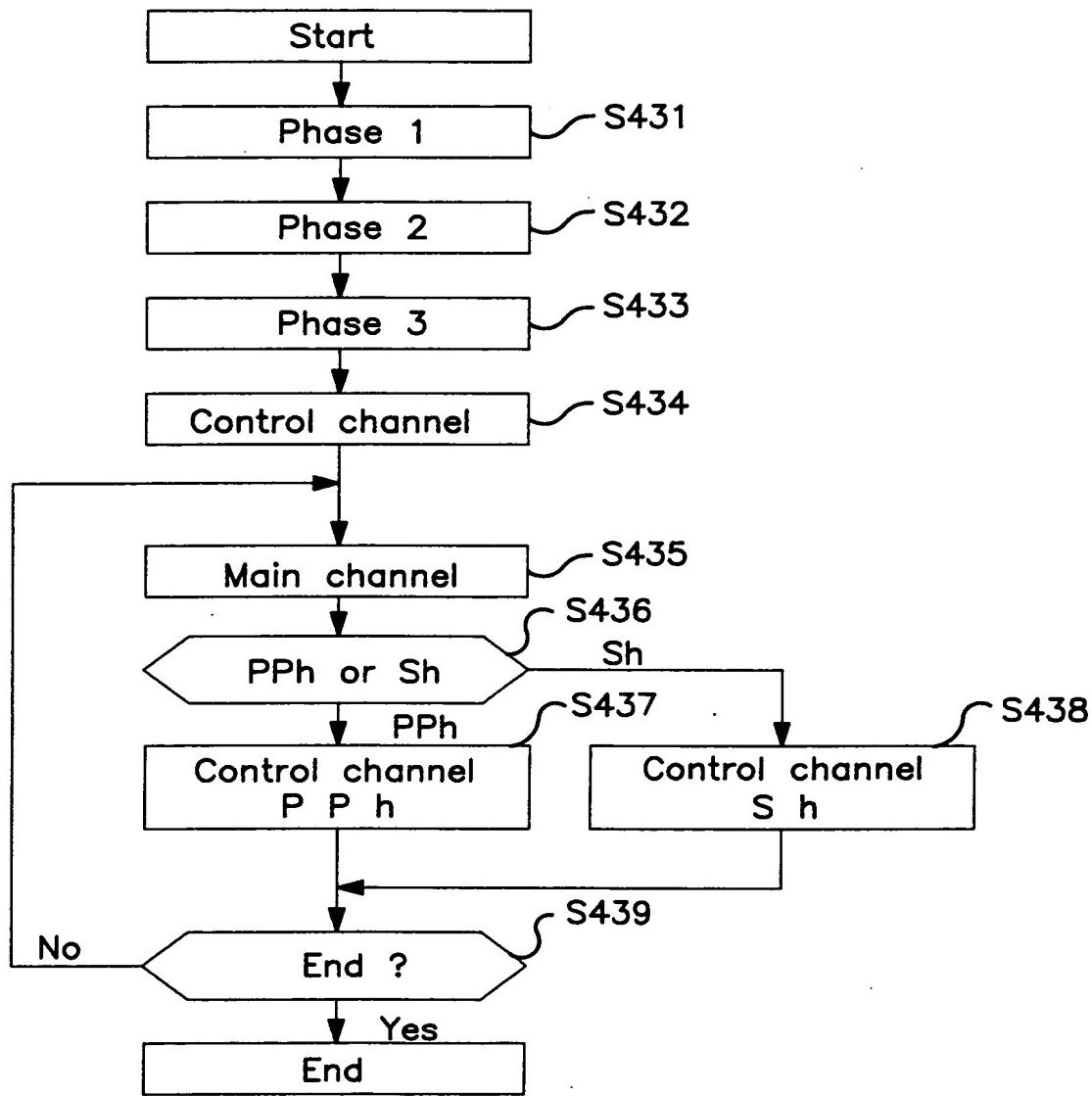
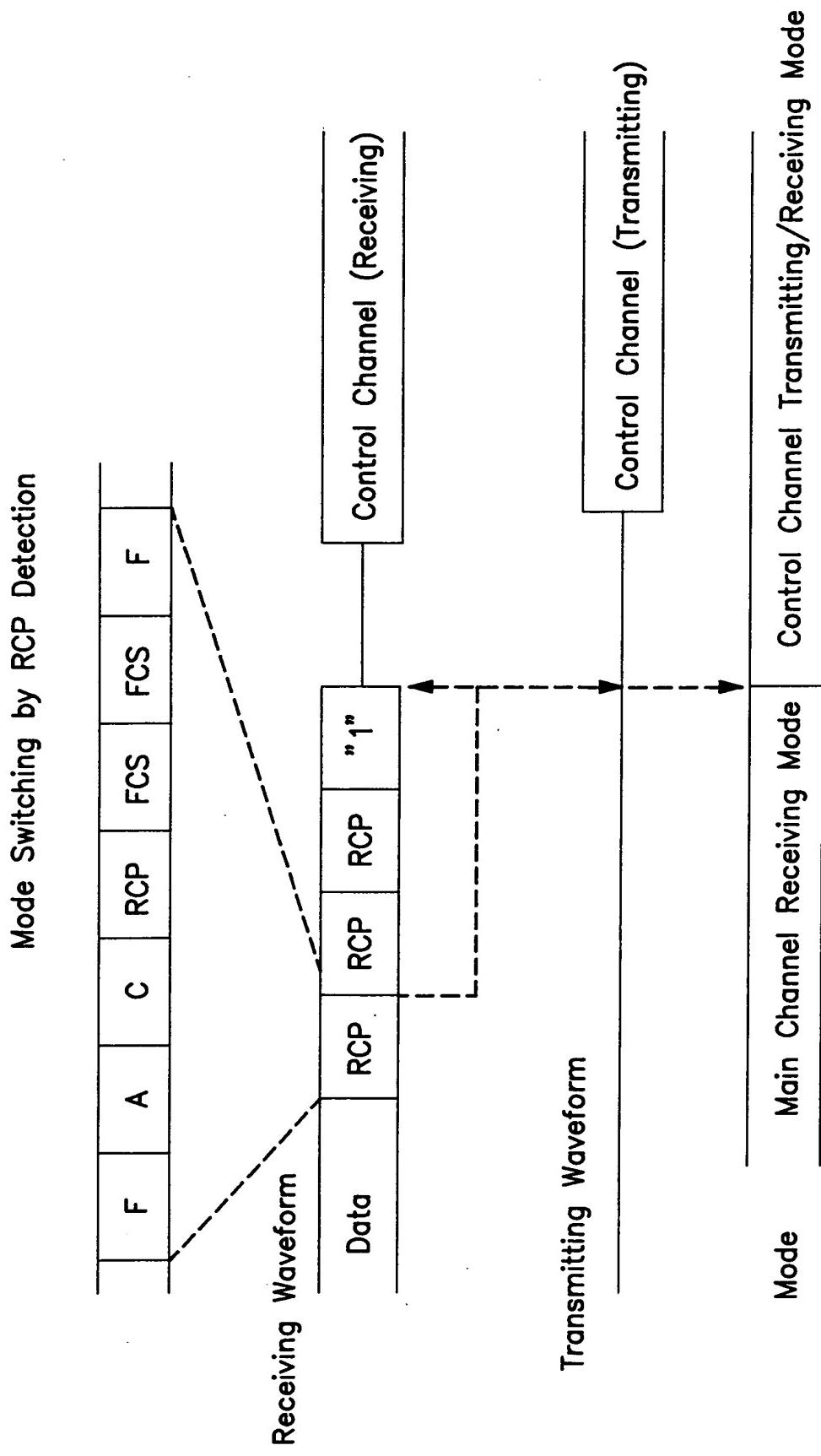


FIG. 16

FIG. 17



Mode Switching by Control-channel-ending-signal

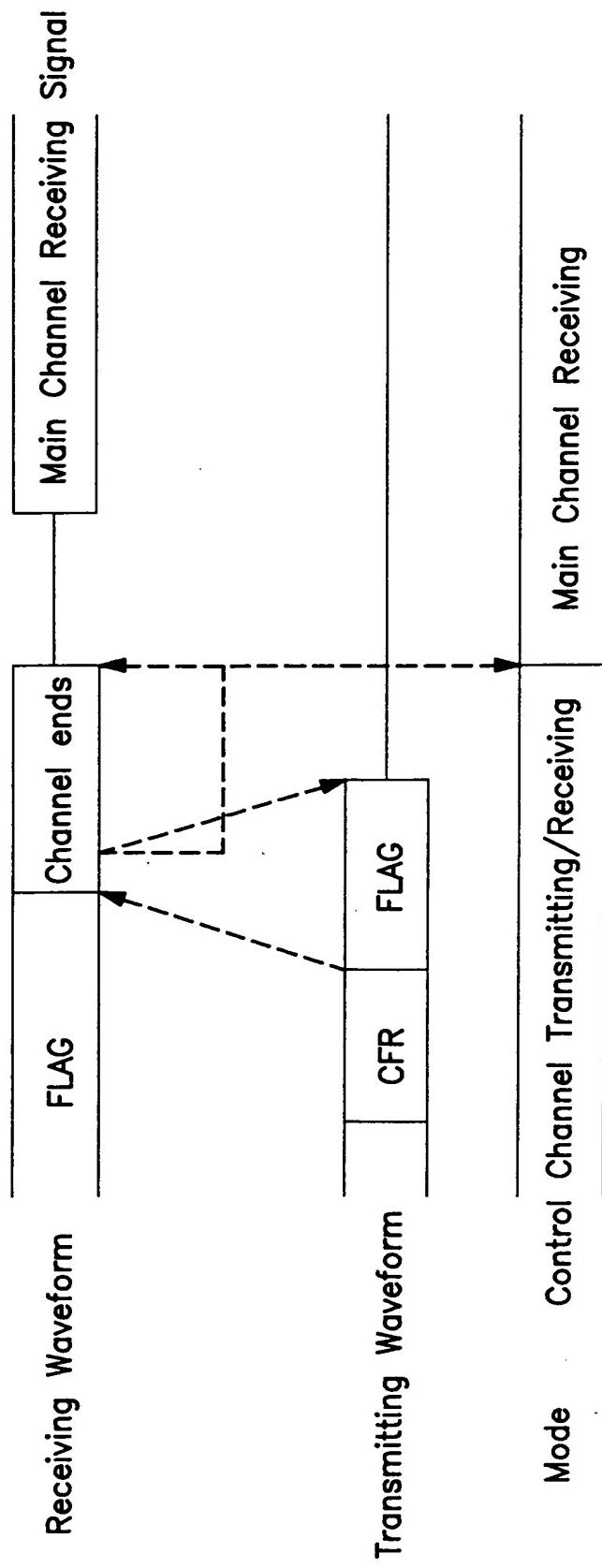
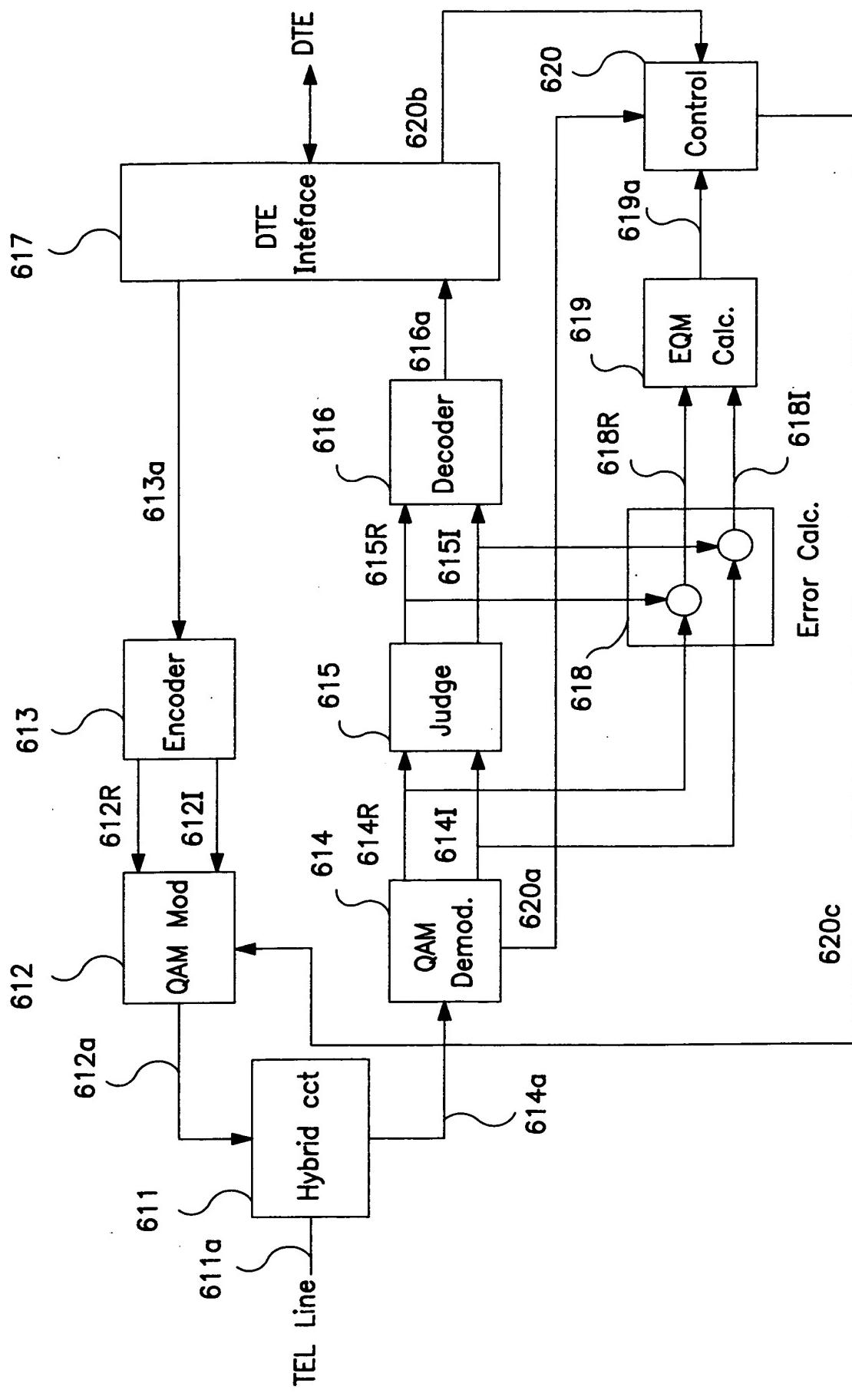


FIG. 18

FIG. 9



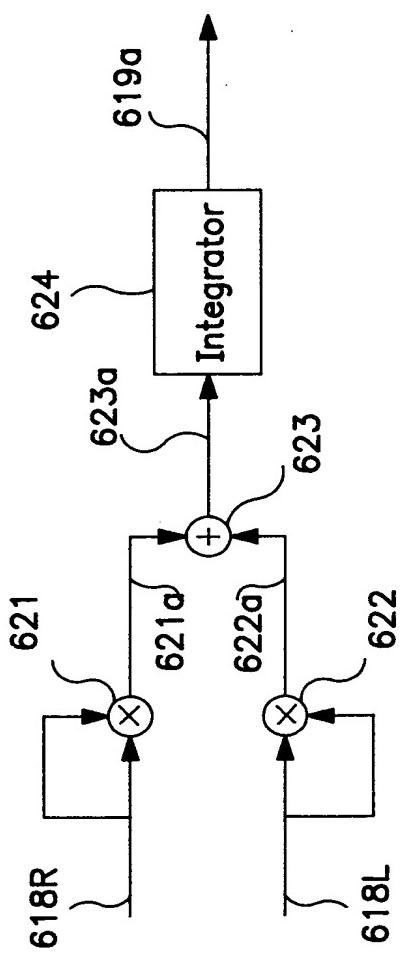


FIG. 20

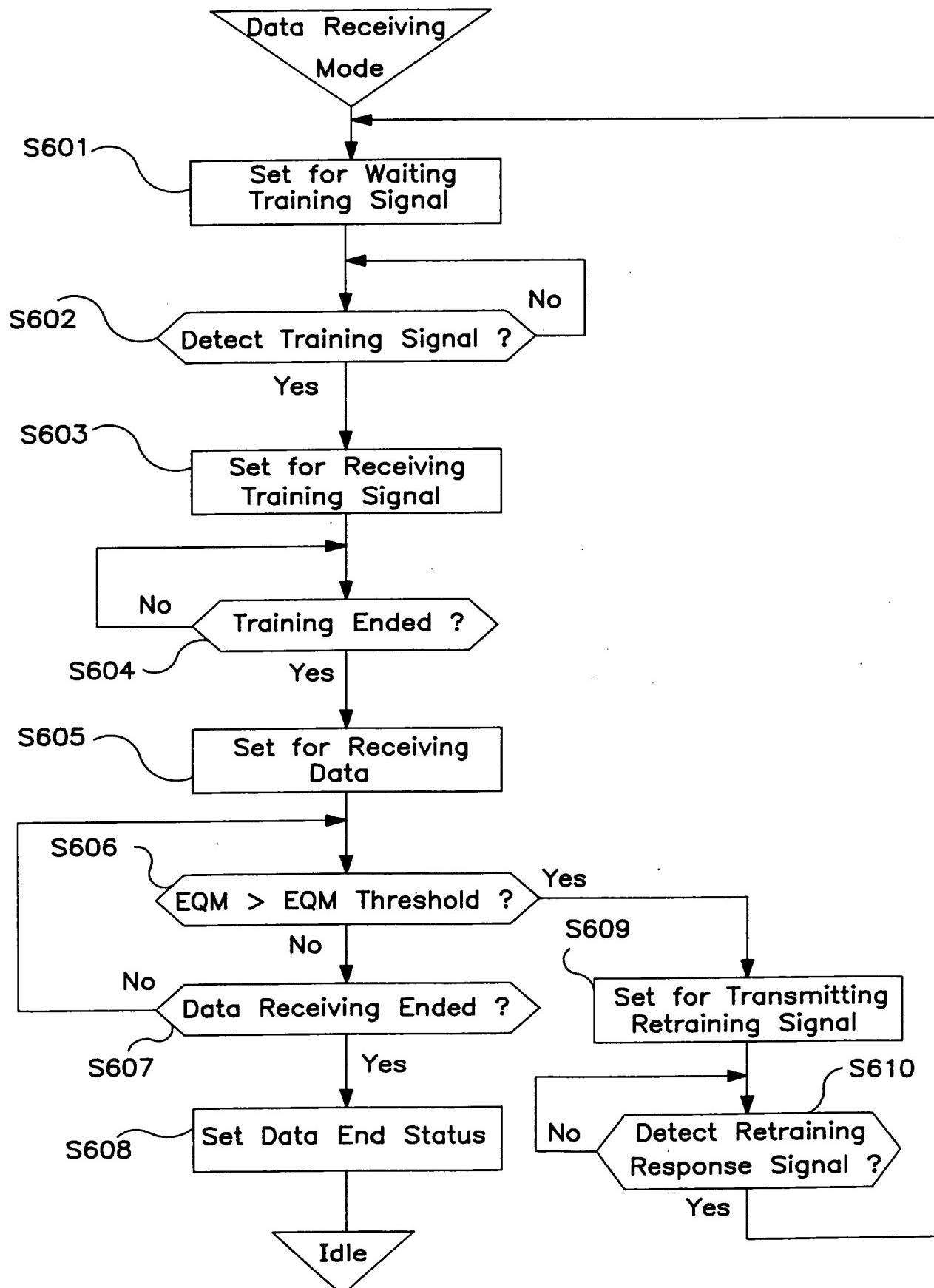


FIG. 21

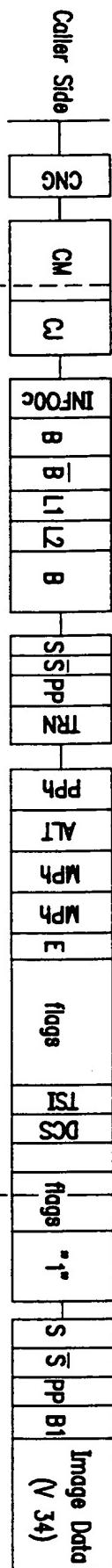
Transmitting
Mode

V34. Facsimile Start Up Procedure

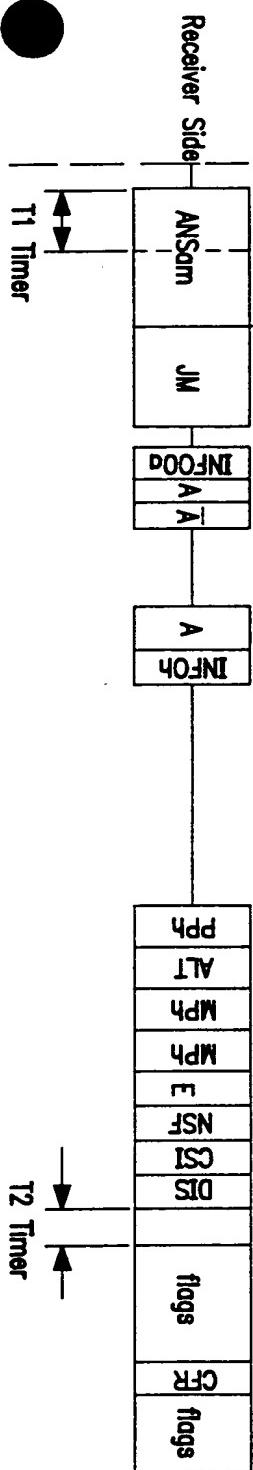
V34. Caller Side Mode

T1 Timer

T2 Timer



Receiver Side



V34. Receiver Side Mode

T1 Timer

T2 Timer

FIG. 22